Assignment no 7: Chapter 7

Note: You can check the exercises after the book Chapter. In our assignment, we are using the 11th edition of "Digital Fundamentals" By Thomas L. Floyd"

2. Solve problem 1 for the input waveforms in Figure 7–71 applied to an active-LOW $\overline{S}$ – $\overline{R}$ latch.

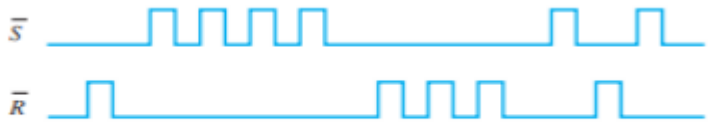


FIGURE 7–71

4. For a gate S – R latch, **Determine** the Q and $\overline{Q}$ outputs for the inputs in Figure 7–73. **Show** them in proper relation to the enable input. Assume the Q starts LOW.

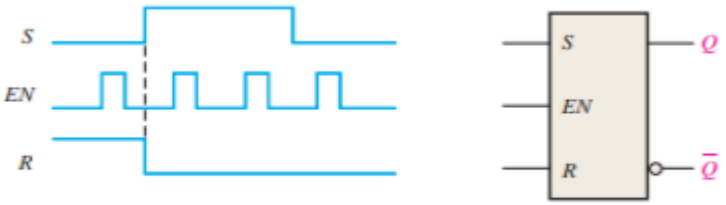


FIGURE 7–73

6. Determine the output of a gated D latch for the inputs in Figure 7–75.

FIGURE 7–75

8. Tow edge-triggered J-K flip-flops are shown in Figure 7–77. If the inputs are as shown, **Draw** the Q output of each flip-flop relative to the clock, and **Explain** the difference between the two.

The flip-flops are initially RESET.

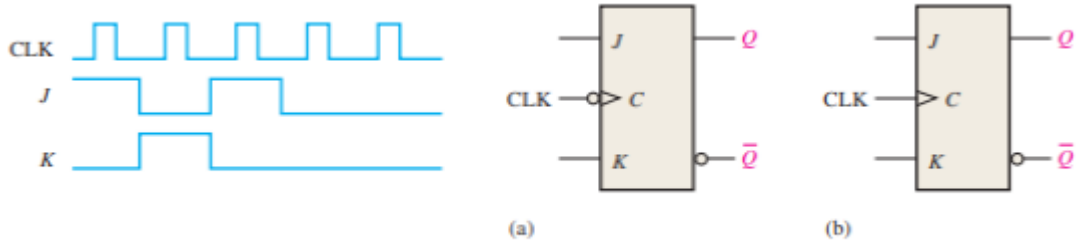


FIGURE 7–77

10. Draw the Q output relative to the clock for a D flip-flop with the inputs as shown in Figure 7–79. Assume positive edge-triggering and Q initially LOW.

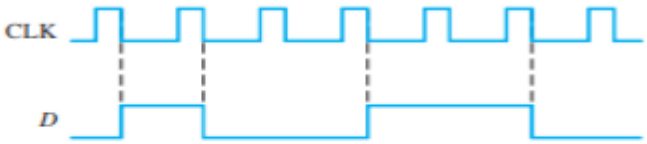


FIGURE 7–79

12. for a positive edge-triggered D flip-flop with the input as shown in Figure 7–81. **Determine** the Q output relative to the clock. Assume that Q starts LOW.

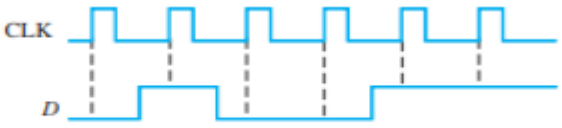
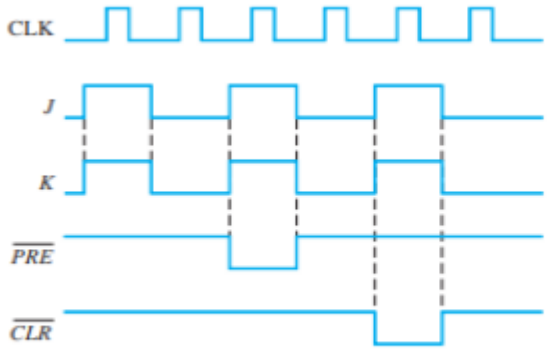


FIGURE 7–81

14. **Determine** the Q waveform relative to the clock if the signals shown in Figure 7–83 are applied to the inputs of the J-K flip-flop. Assume that Q is initially LOW.



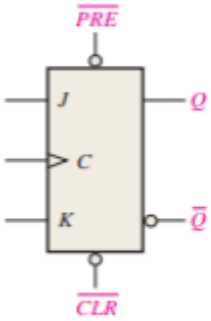


FIGURE 7–83